221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

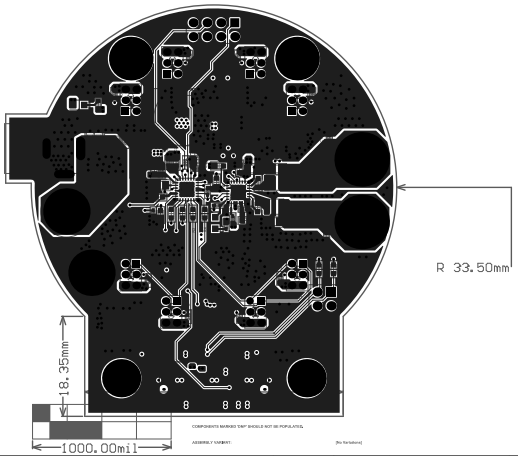
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY+RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION FOR TOP CLOCKS "AND" SIGNALS ENTERPRISED

[unselected-off]

TRANSKY SUBMISSION

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L1_TOP

BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 10/26/2026 3:48:37 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.
222 These assemblies are ESD sensitive, ESD precautions shall be observed.
223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

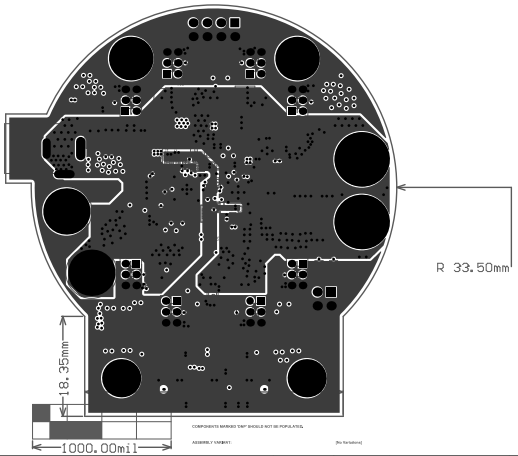
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY+RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION FOR CLOCKWISE ORIENTATION

TRAINING SUBSESSION

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L2-GND1
BOARD #: Robotics Design REV: A SVN REV: Not in version control
DID #: TIDA-060054
GENERATED : 10/26/2026 9:48:28 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.
222 These assemblies are ESD sensitive, ESD precautions shall be observed.
223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

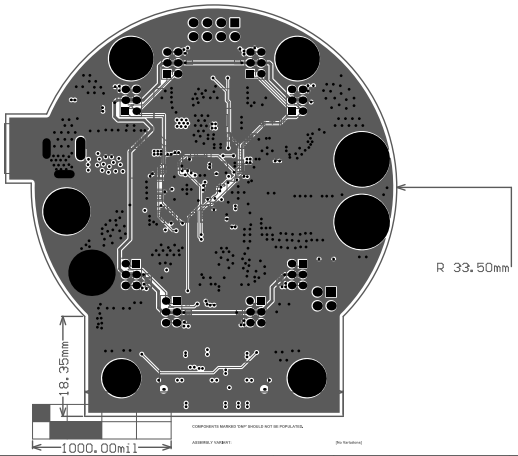
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations] [selected set] TRIMMED TO BOARD

JUSTIFICATION TOP CLOCKWISE BOTTOM CLOCKWISE

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L3_Signal
BOARD #: Robotics Design REV: A SVN REV: Not in version control
3RD #: TIDA-060054
GENERATED : 10/26/2026 3:48:29 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

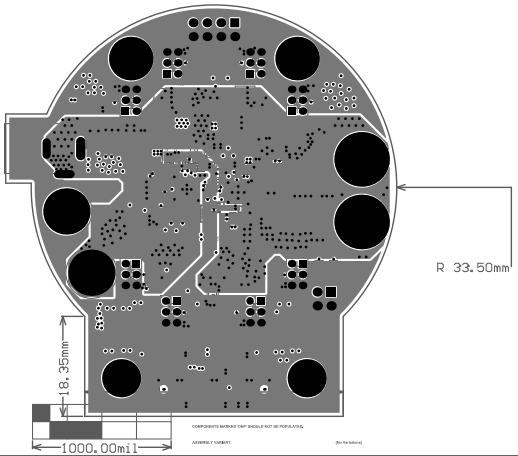
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = L4_GND2
BOARD #: Robotics Design REV: A SVN REV: Not in version control
DID #: TIDA-060054
GENERATED : 10/26/2026 3:48:41 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

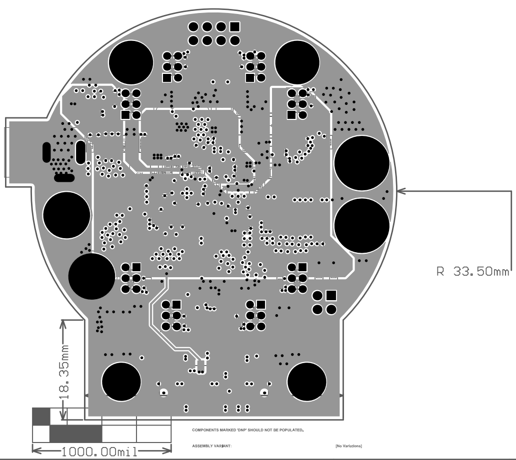
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
BOARD #: Robotics Design REV: A SVN REV: Not in version control
LAYER NAME = Bottom
TID #: TIDA-060054
PLOT NAME = L5_PWR
GENERATED : 10/26/2026 3:48:42 PM TEXAS INSTRUMENTS

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IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

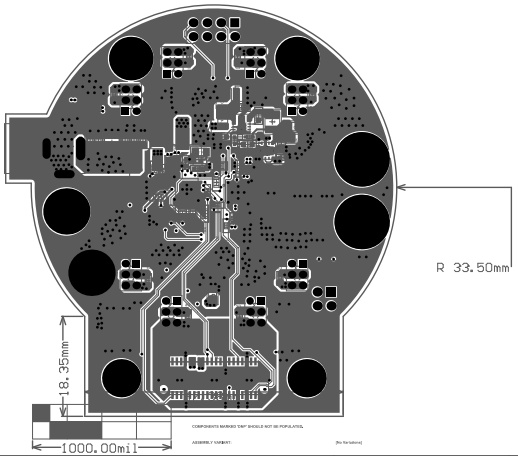
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Bottom
PLOT NAME = L6_Bottom
BOARD #: Robotics_Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 3:48:43 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

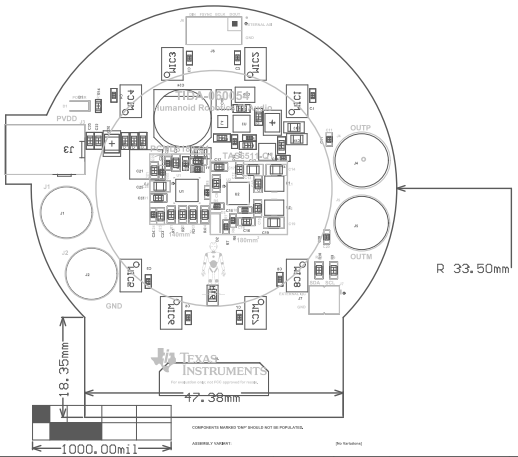
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
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TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Top
PLOT NAME = Top Silkscreen Overlay
BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 10/26/2026 3:48:44 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

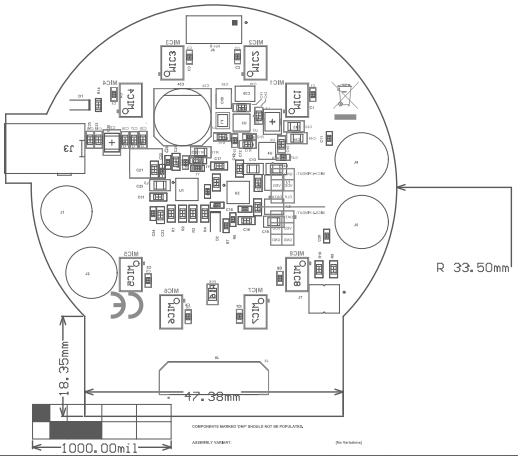
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
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TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Bottom Silkscreen Overlay

BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 9:48:46 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221	■	Board sized to silkscreened box after final mods. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.	
222	■	These assemblies are ESD sensitive, ESD precautions shall be observed.	
223	■	These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.	
224	■	These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.	

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
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	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

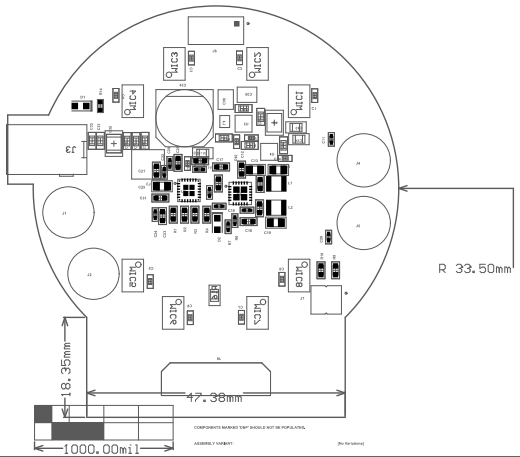
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
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TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
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MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations] [selection ref] TRANSKY SUBSTRATE

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

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PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
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TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics Design REV: A SVN REV: Not in version control
LAYER NAME = Top Solder, Bottom	IID #: TIDA-060054
PLOT NAME = Top Paste, Mask Print	GENERATED : 10/26/2026 3:48:47 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey	LAYOUT BY: Tessolve
SCALE: 0.72	ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

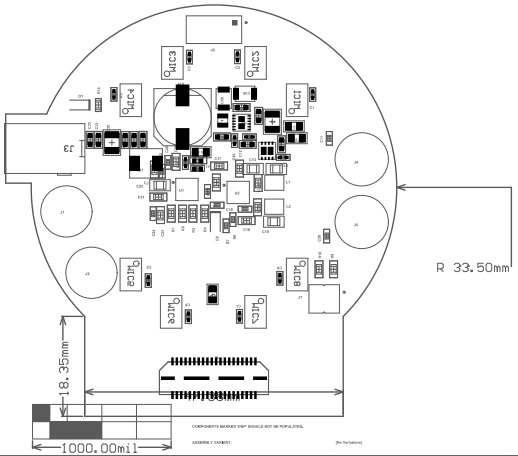
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION			
MIN. TRACK WIDTH:	5 MIL		
MIN. CLEARANCE:	6 MIL		
MIN. VIA PAD SIZE:	19.685 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES	+/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics_Design REV: A SVN REV: Not in version control
LAYER NAME = Bottom	TID #: TIDA-060054
PLOT NAME = Bottom Paste Mask Print	GENERATED : 10/26/2026 3:48:48 PM TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Garret Godfrey	Tessolve
SCALE: 0.72	ALTIUM DESIGNER VERSION: 23.1.1.15

221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

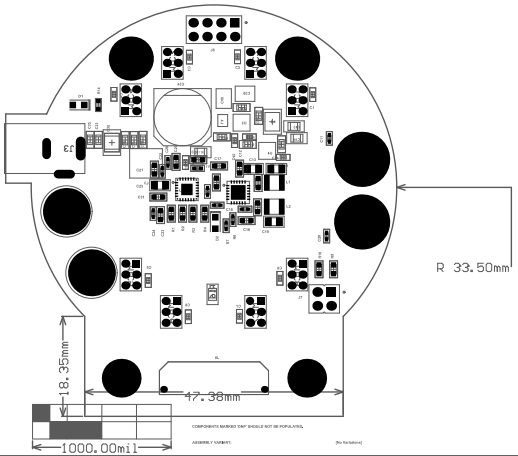
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations] [working/out-of] TRANSKIT SUBMISSION

JUSTIFICATION FOR CLOSURE "WHO" DOMAIN EXPERIENCED

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Top Solder Mask Top Bottom
PLOT NAME = Top Solder Mask Print

BOARD #: Robotics Design REV: A SVN REV: Not in version control
3RD MOTTOO MOFI EDROM BOM
3RD #: TIDA-060054
GENERATED : 10/26/2026 3:48:49 PM
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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 Board sized to silkscreened box after final mask. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

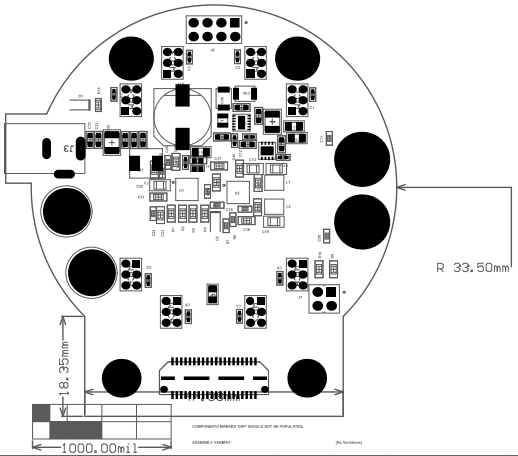
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION FOR CLOSING THIS VERSION STEP/DRAWING

DESIGN INFORMATION			
MIN. TRACK WIDTH:	5 MIL		
MIN. CLEARANCE:	6 MIL		
MIN. VIA PAD SIZE:	19.685 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES	+/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = Bottom

PLOT NAME = Bottom Solder Mask Print

BOARD #: Robotics_Design REV: A SVN REV: Not in version control

IID #: TIDA-060054

GENERATED : 10/26/2026 3:48:50 PM

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ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

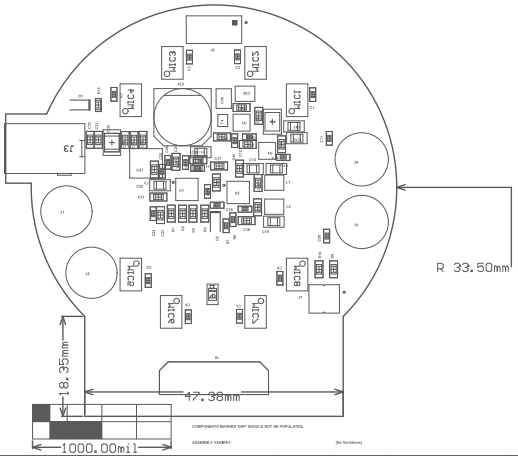
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0,05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M1 Board Outline
BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 9:48:52 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Install steel to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

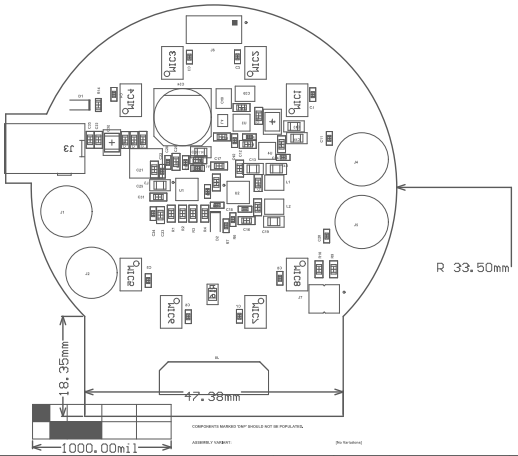
LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				
Total board thickness:			68.00mil		+/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION FOR TOP CLOCKS "PAD" DOMAIN OVERSPOKED

TRAINING SUBMISSION

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M2 Board Dimensions

BOARD #: Robotics Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 9:48:53 PM
TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

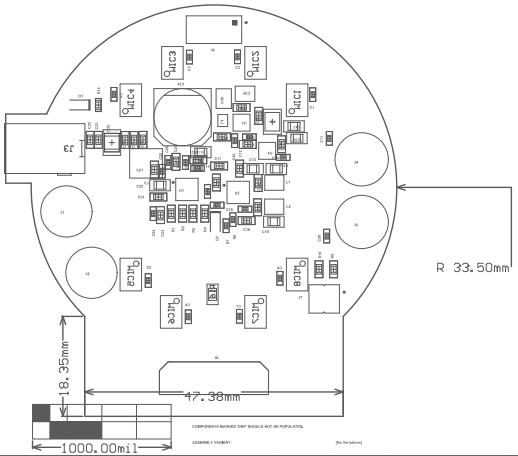
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 Board sized to silkscreened box after final route. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION TOP CLOCKWISE *AND CENTER-STRAIGHTFORWARD

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M3 3D STEP Top

BOARD #: Robotics Design REV: A SVN REV: Not in version control
STD #: TIDA-060054
GENERATED : 10/26/2026 9:48:54 PM TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to allow removal less after final mask. Test shall be 5 pt here. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

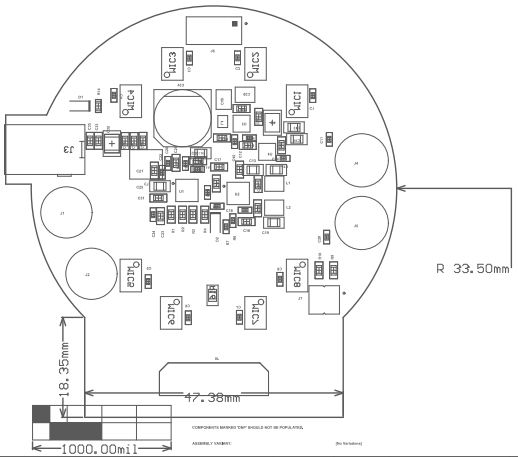
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M4 3D STEP Bottom
BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 3:48:55 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

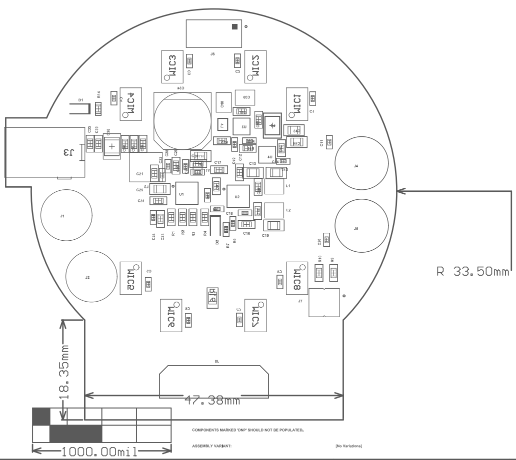
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics Design	REV: A	SVN REV: Not in version control
LAYER NAME = [illegible]	TID #: TIDA-060054		
PLOT NAME = M5 Assembly Top	GENERATED : 10/26/2026	3:48:56 PM	TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to silkscreened box after final route. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
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	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

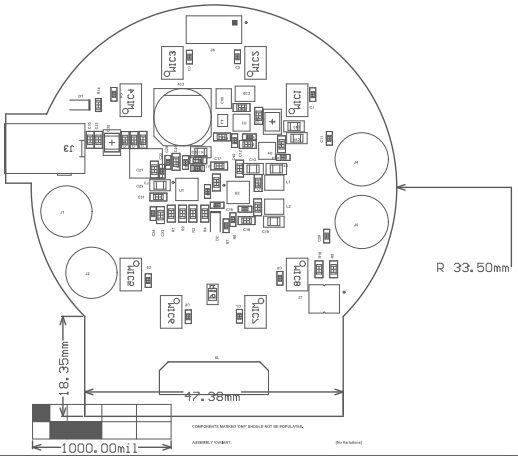
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted] Bottom
PLOT NAME = M6 Assembly Bottom
BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 9:48:57 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

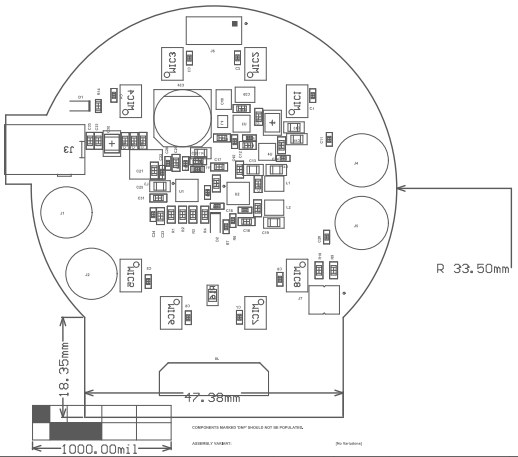
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Bottom
PLOT NAME = MsTitle Sheet
BOARD #: Robotics_Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 9:48:09 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

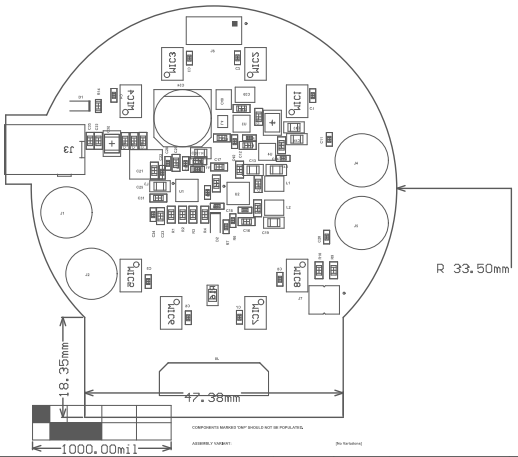
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations] [selection ref] TRANSKY SUBMISSION

JUSTIFICATION TOP CLOCKWISE BOTTOM COUNTERCLOCKWISE

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M10 Fab Notes

BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 3:48:00 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

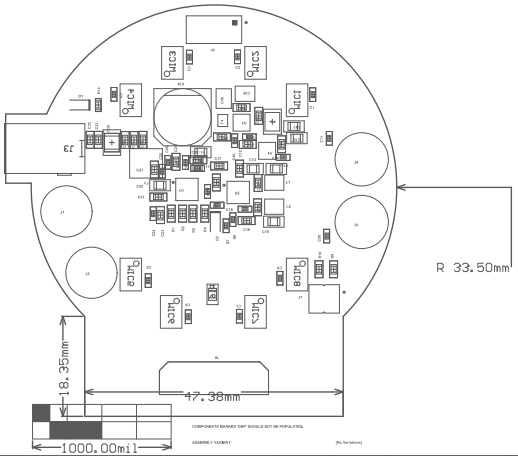
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Mid_GerberInformation
BOARD #: Robotics_Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 9:48:02 PM
TEXAS INSTRUMENTS

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221 ■ Install shield to silkscreened box after final wash. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

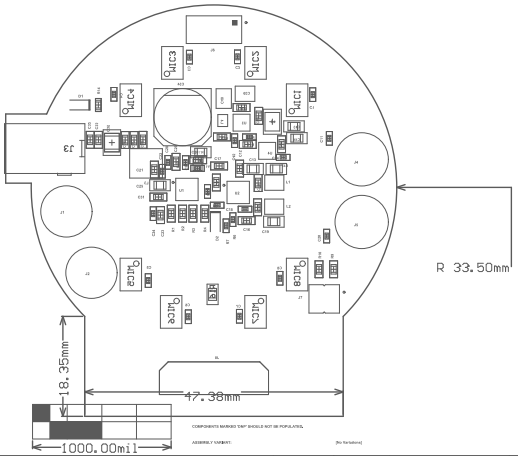
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M12 Stackup
BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 3:48:02 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to allow overall size after final mask. Test shall be 8 pt here. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

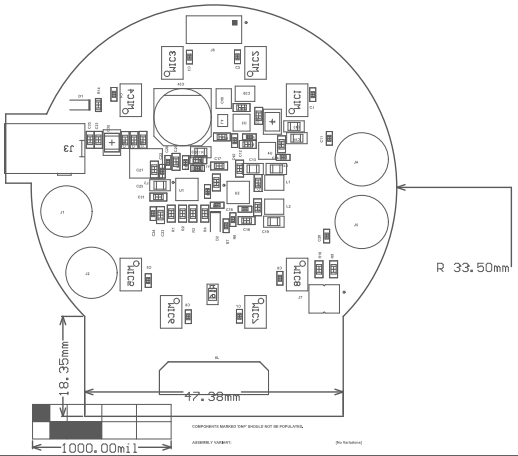
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M13 Component Bodies Top
BOARD #: Robotics Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 3:48:03 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221	Bevel used to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.		
222	These assemblies are ESD sensitive, ESD precautions shall be observed.		
223	These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.		
224	These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.		

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

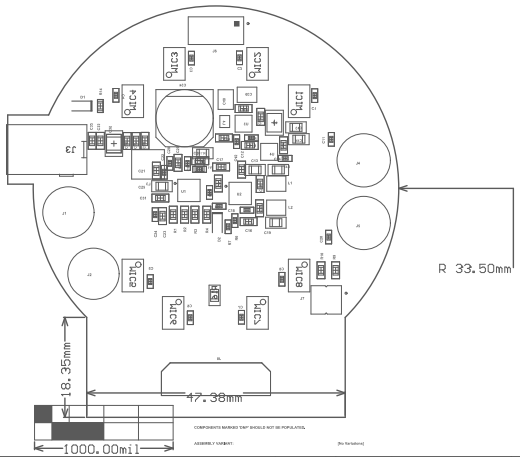
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

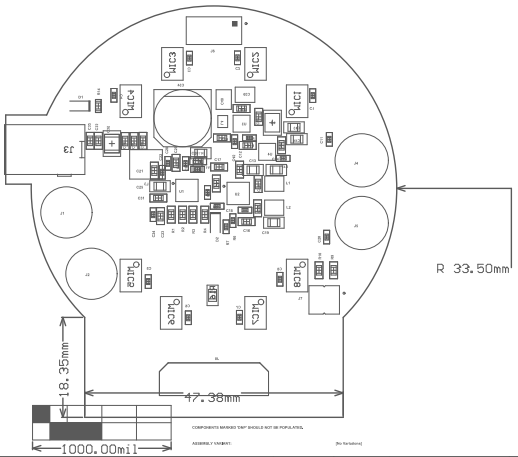
ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M14 Component Bodies Bottom

BOARD #: Robotics Design REV: A SVN REV: Not in version control
SID #: TIDA-060054
GENERATED : 10/26/2026 3:49:04 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Board sized to allow removal less after final mask. Test shall be 5 pt here. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

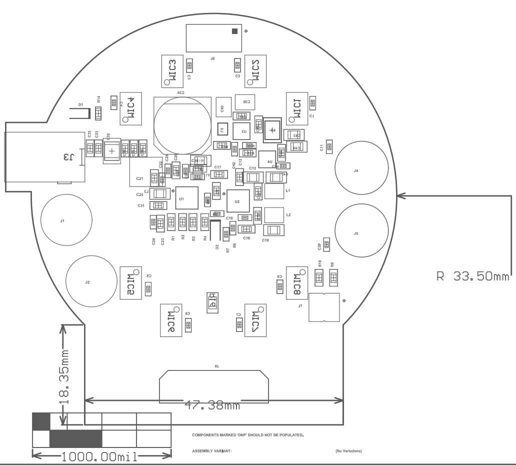
TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M4S Courtyards Top
BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 10/26/2026 9:48:05 PM
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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15



ZZ1 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.80mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.80mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1. THIS IS IMPEDANCE CONTROLLED BOARD.
2. ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED . PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA TENTING / COVERING " REQUIREMENTS.
4. 7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES . MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc
ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE		BOARD #: Robotics Design	REV: A	SVN REV: Not in version control	
LAYER NAME = [illegible]		TID #: TIDA-060054			
PLOT NAME = M16 Courtyards Bottom		GENERATED : 10/26/2026	3:49:07 PM	TEXAS INSTRUMENTS	

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1	2	3	4	5	6

221 ■ Board sized to silkscreened box after final mods. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.
222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

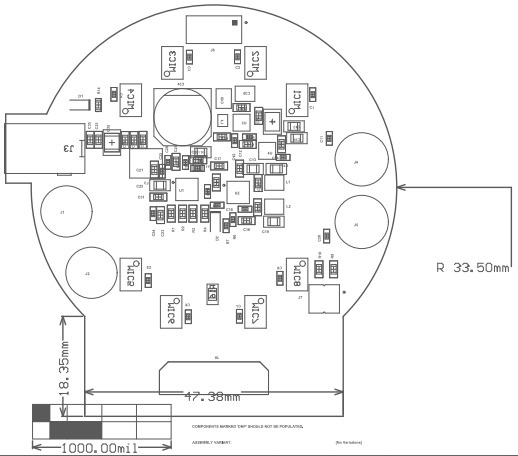
STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.
2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.
3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.
4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M17 Embedded Cavity

BOARD #: Robotics Design REV: A SVN REV: Not in version control
3RD MOTTO MOFI EDROM BOM
3RD #: TIDA-060054
GENERATED : 10/26/2026 3:48:08 PM
TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

1	2	3	4	5	6

221 ■ Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

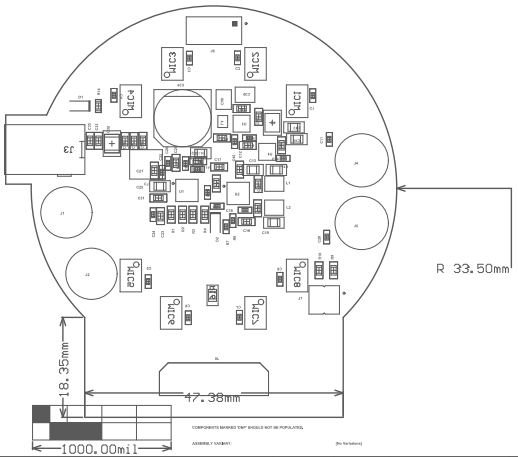
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = M48 Embedded Assembly
BOARD #: Robotics Design REV: A SVN REV: Not in version control
IID #: TIDA-060054
GENERATED : 10/26/2026 9:49:09 PM
TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 Bevel sized to silkscreened text after final mask. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

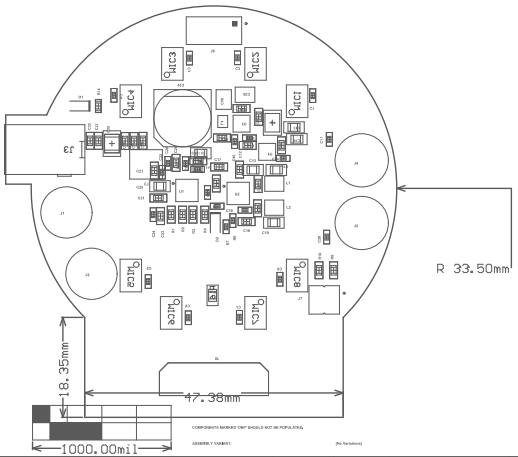
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION TOP CLOCKWISE *AND CENTER OTHERWISED

DESIGN INFORMATION			
MIN. TRACK WIDTH:	5 MIL		
MIN. CLEARANCE:	6 MIL		
MIN. VIA PAD SIZE:	19.685 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES	+/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = M4G Embedded Keepout

BOARD #: Robotics Design REV: A SVN REV: Not in version control

IID #: TIDA-060054

GENERATED : 10/26/2026 9:49:10 PM

TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

221 Board sized to silkscreened box after final route. Tool shall be 0 pt here. Tool shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

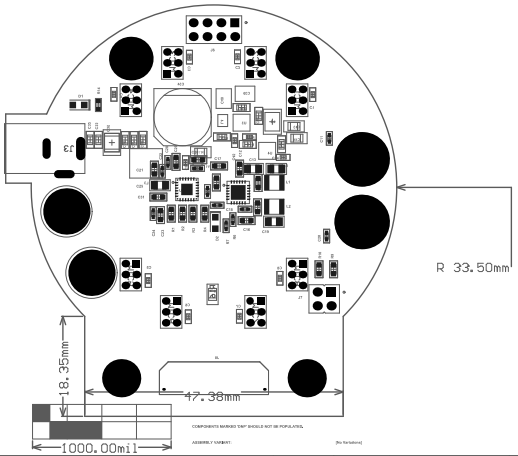
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER. SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION: BE TOP CLICKING "FREE" DOMAIN ENTERPRISED

DESIGN INFORMATION	
MIN. TRACK WIDTH:	5 MIL
MIN. CLEARANCE:	6 MIL
MIN. VIA PAD SIZE:	19.685 MIL
MINIMUM ANNULAR RING	0.05mm (2MIL) EXTERNAL
PER	IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: Robotics_Design REV: A SVN REV: Not in version control
LAYER NAME = [redacted]Bottom	TID #: TIDA-060054
PLOT NAME = Top Pad Master	GENERATED : 10/26/2026 3:49:41 PM TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Garret Godfrey	Tessolve
SCALE: 0.72	ALTIUM DESIGNER VERSION: 23.1.1.15

221 Board sized to allow normal box after final mask. Test shall be 5 pt box. Test shall be per the Label Table in the PDF schematic.

222 These assemblies are ESD sensitive, ESD precautions shall be observed.

223 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

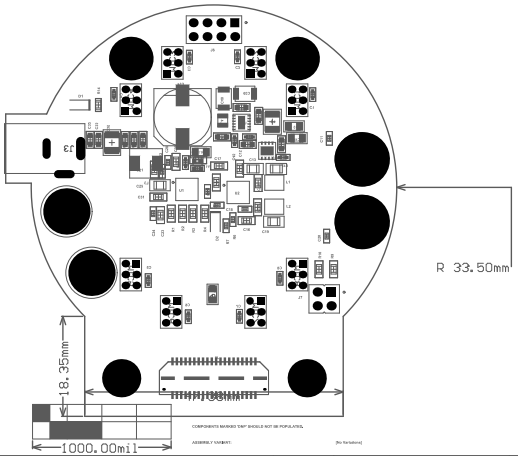
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

SOLDERMASK TO TOP CLOSING "PAD" DOMAIN EVERYWHERE

DESIGN INFORMATION			
MIN. TRACK WIDTH:	5 MIL		
MIN. CLEARANCE:	6 MIL		
MIN. VIA PAD SIZE:	19.685 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES	+/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = [redacted]Bottom
PLOT NAME = Bottom Pad Master
BOARD #: Robotics Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 3:49:13 PM TEXAS INSTRUMENTS

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

221 ■ Install shall be silkscreened face after final wash. Text shall be 5 pt font. Text shall be per the Label Table in the PDF schematic.

222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

223 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

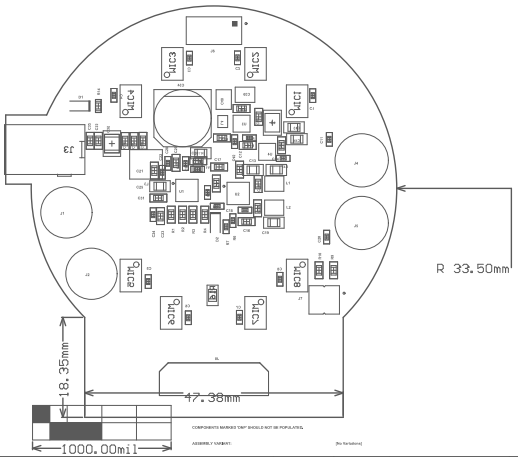
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
AS PER THE MANUFACTURING CAPABILITIES AND ALL OTHER SOLDER MASK PADS SHALL NOT BE MODIFIED .
PROVIDED NO ADJACENT COPPER IS EXPOSED AND NO CONFLICT IS PRODUCED WITH ANY STATED " VIA
TENTING / COVERING " REQUIREMENTS.

4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

JUSTIFICATION TOP CLOCKWISE *AND CENTER ENTERPRISED

DESIGN INFORMATION			
MIN. TRACK WIDTH:	5 MIL		
MIN. CLEARANCE:	6 MIL		
MIN. VIA PAD SIZE:	19.685 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL, HOLES	+/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design

DESIGNED FOR: TI Internal

FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = Keep Out Layer

BOARD #: Robotics Design REV: A SVN REV: Not in version control

IID #: TIDA-060054

GENERATED : 10/26/2026 3:48:14 PM

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ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

DRILL TABLE

Symbol	Count	Hole Size	Plated	Hole Type
	13	7.87mil (0.200mm)	PTH	Round
	509	10.00mil (0.254mm)	PTH	Round
	2	29.92mil (0.760mm)	PTH	Slot
	48	35.04mil (0.890mm)	PTH	Round
	2	39.37mil (1.000mm)	NPTH	Round
	1	39.76mil (1.010mm)	PTH	Slot
	8	40.00mil (1.016mm)	PTH	Round
	4	47.24mil (1.200mm)	PTH	Round
	2	126.00mil (3.200mm)	PTH	Round
	2	129.92mil (3.300mm)	PTH	Round
	2	144.00mil (3.658mm)	PTH	Round
	2	214.57mil (5.450mm)	PTH	Round
	595 Total			

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position,
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

FOR 7.87 MIL DRILL +0/-7.87MIL

FOR 10 MIL DRILL +0/-10 MIL

FOR NPTH +/- 2MIL

FOR PTH +/- 3MIL

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
	TRACE WIDTH	REFERENCE
L1	6.5 MILLS	L2
L3	5 MILLS	L2&L4
L6	6.5 MILLS	L5

STACK UP

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.20mil	3.5	
1	L1_TOP	Copper	1.20mil		
	Dielectric 1	FR-4	4.60mil	4	
2	L2-GND1	copper	1.40mil		
	Dielectric 2	FR-4	4.00mil	4	
3	L3_Signal	copper	1.40mil		
	Dielectric 3	FR-4	39.20mil	4	
4	L4_GND2	copper	1.40mil		
	Dielectric 4	FR-4	4.00mil	4	
5	L5_PWR	copper	1.40mil		
	Dielectric 5	FR-4	4.60mil	4	
6	L6_Bottom	Copper	1.20mil		
	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

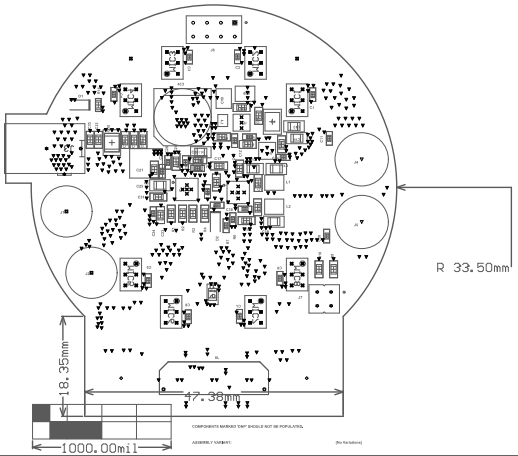
FAB NOTES

1.THIS IS IMPEDANCE CONTROLLED BOARD.

2.ALL VIAS ARE TENTED IN BOTH SIDE UNLESS OTHERWISE MASK OPENED IN GERBERS.

3.VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1)
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4.7.874 MILS VIAS NEED TO BE FILLED WITH NON CONDUCTIVE EPOXY-RESIN AND OVERPLATE
WITH COPPER, SURFACE MUST BE FLAT, FLATNESS TOLERANCE IS +0.000/-0.001" ON TOP SIDES .
MINIMUM ANNULAR RING REQUIREMENT IS WAIVED FOR FILLED VIAS.



DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 19.685 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[X] FR-4 [ ] FR-4 High Tg [ ] OTHER
THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
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[X] RoHS [ ] OTHER PER ORDER

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ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Robotics Design
DESIGNED FOR: TI Internal
FILE NAME: Robotics_Design.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE
LAYER NAME = Drill Drawing For (L1_TOP • L6_Bottom)
PLOT NAME = Drill Drawing For (L1_TOP • L6_Bottom)

BOARD #: Robotics_Design REV: A SVN REV: Not in version control
TID #: TIDA-060054
GENERATED : 10/26/2026 9:48:15 PM

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ENGINEER: Garret Godfrey
LAYOUT BY: Tessolve
SCALE: 0.72
ALTIUM DESIGNER VERSION: 23.1.1.15

IMPEDANCE TABLE:

LAYERS	50 OHM SIGNAL +/- 10% Tolerance	
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STACK UP

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	Bottom Solder	Solder Resist	1.20mil	3.5	
	Bottom Overlay				

Total board thickness: 68.00mil +/-10%

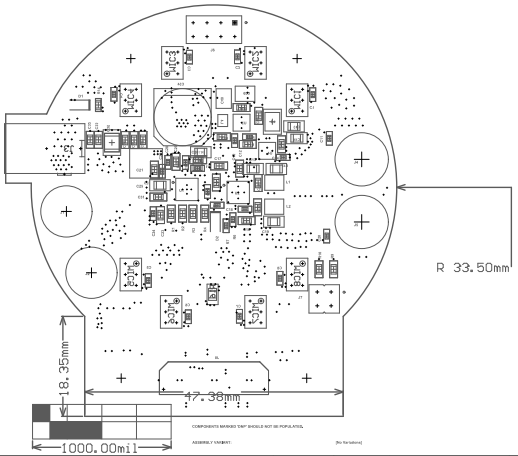
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DESIGN INFORMATION

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MIN. CLEARANCE: 6 MIL

MIN. VIA PAD SIZE: 19.685 MIL

MINIMUM ANNULAR RING 0,05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[X] FR-4 [ ] FR-4 High Tg [ ] OTHER

THICKNESS: [ ] 62 MIL (1.6mm) +/-10% [X] OTHER Refer stack up

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [X] GREEN [ ] OTHER

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG

[ ] IMM- TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [ ] V. SCORE

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ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

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DESIGNED FOR: TI Internal

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ENGINEER: Garret Godfrey

LAYOUT BY: Tessolve

SCALE: 0.72

ALTIUM DESIGNER VERSION: 23.1.1.15

ALL ARTWORK VIEWED FROM TOP SIDE

LAYER NAME = [redacted]Bottom

PLOT NAME = Drill Guide For (L1_TOP - L6_Bottom)

BOARD #: Robotics Design REV: A SVN REV: Not in version control

TID #: TIDA-060054

GENERATED : 10/26/2026 3:48:17 PM

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